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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,379	07/08/2002	W. Riyon Harding	BUR920010179	4016
28722	7590	09/08/2004	EXAMINER	
BRACEWELL & PATTERSON, L.L.P.			DALEY, CHRISTOPHER ANTHONY	
P.O. BOX 969			ART UNIT	
AUSTIN, TX 78767-0969			PAPER NUMBER	
			2111	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/064,379

Applicant(s)

HARDING ET AL.

Examiner

Christopher A Daley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5 and 13 is/are allowed.
- 6) ☒ Claim(s) 1-4,6-12,14-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/08/22002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 07/08/2002.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 16 are pending

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen et al (US6073199), hereafter Cohen.

4. As to claims 1 and 9, Cohen discloses an apparatus and method for providing bus arbitrations in a multiprocessor system, said apparatus comprising: a bus request history table for storing a history of bus requests for a system bus made by a plurality of cores, where said system bus is shared by said plurality of cores; (Figure 1 displays a computer system 12 with a system bus 20, coupled to a CPU 14, and other processor device such as network controller 32, and storage controller 36, COL. 3, lines 41 – 46). and control logic 44 providing the arbiter function, coupled to said bus request history table, for arbitrating said system bus among said plurality of cores in response to bus requests made by said plurality of cores, according to information stored in said bus request history table. (Figure 1 displays an arbiter 28, coupled to system bus 20. Arbiter 28 comprises arbitration control logic 44 and a history table 48, Figure 2).

5. As to claims 2 and 10, Cohen discloses the apparatus and method, where said bus request history table includes a current bus owner column, a next bus owner column, and a number of misses column. (Cohen teaches in Figure 3 several cases of the arbiter history. In case 1 for example, Cohen shows the history queue with the current owner of the bus, M3, the prior owner of the bus M2, (Col. 4, lines 45 – 46). As far as the next bus owner is concerned, Cohen teaches of a hidden arbitration scheme of choosing the next bus master for the next available cycle, (COL. 2, lines 25 – 28). The arbiter also monitors for aborted bus transactions, thus keep count of the misses, (COL. 2, lines 8 – 11).

6. As to claims 3 and 11, Cohen discloses the apparatus of claim 2 and the method, where said arbiter, in response to a bus request from a core having an entry in said current bus owner column, automatically grants said system bus to a core according to a corresponding entry in said next bus owner column after said bus request. (Cohen teaches the usage of a history based arbitration scheme in combination with other priority schemes such as granting a device super priority. This would allow for this device to be chosen by the hidden arbitration scheme and be awarded the bus grant, COL. 5, lines 15 – 24).

7. As to claims 4 and 12, Cohen discloses the apparatus and method, where said bus request history table is implemented by a cache memory. (Cohen teaches that his arbiter that contains the history table can be implemented in discrete logic, (COL. 2,

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lines 65 – 67). Cohen also teaches that his invention can be modified in arrangement and detail while maintaining the spirit of the invention (COL. 7, lines 41 – 46). Using cache memory would be evident to one of ordinary skill in the art for the history table storage element),

8. As to claims 6 and 14, Cohen discloses the apparatus and method, where said arbiter, in response to bus requests from a sequence of cores having an entry in said processor sequence column, automatically grants said system bus to a sequence of cores according to a corresponding entry in said next sequence number column after said bus requests. (Cohen teaches that the arbiter can impose implicit priorities thus overriding the history queue. The arbiter can be programmed to favor a certain device bus grant sequence, COL. 4 line 66 – COL. 5, line 7).

9. As to claims 7 and 15, Cohen discloses the apparatus and method, where said bus request history table is implemented by content-addressable memory. (Cohen teaches that his arbiter that contains the history table can be implemented in discrete logic, (COL. 2, lines 65 – 67). Cohen also teaches that his invention can be modified in arrangement and detail while maintaining the spirit of the invention (COL. 7, lines 41 – 46). Using content-addressable memory would be evident to one of ordinary skill in the art for the history table storage element),

10. As to claims 8 and 16, Cohen discloses the apparatus and method, where said core is a processor. (Cohen teaches that said core is a CPU, 14 in Figure 1, COL. 3, lines 41 – 43).

Allowable Subject Matter

Claims 5 and 13 are allowable over the prior of records.

Claims 5 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner's Statement of Reasons for Allowance

1. Claims 5 and 13 are allowable over the prior of records.
2. Claims 5 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
3. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 5 and 13 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts. Prior art fails to teach an apparatus and a method, where said bus request history table includes a current sequence number column, a processor sequence column, a next sequence number column, and a number of misses column.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A Daley whose telephone number is 703 605 4214. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD

CAD
August 25, 2004



TMVO
PRIMARY EXAMINER